

IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

2

Attorney Docket No.: Poly-19/APP

Applicants: Hung-Hsiang Jonathan CHAO, Eiji OKI

Serial No.: 09/872,892

Filing Date: June 1, 2001

Title: SCHEDULING THE DISPATCH OF CELLS IN MULTISTAGE SWITCHES
USING A HIERARCHICAL ARBITRATION SCHEME FOR MATCHING
NON-EMPTY VIRTUAL OUTPUT QUEUES OF A MODULE WITH OUTGOING
LINKS OF THE MODULE

Examiner: Not yet assigned

Group Art Unit: Not yet assigned

Assistant Commissioner for Patents
BOX PATENT APPLICATION
Washington, D.C. 20231

S I R:

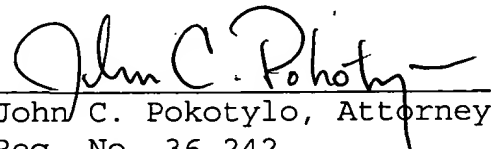
Information Disclosure Statement

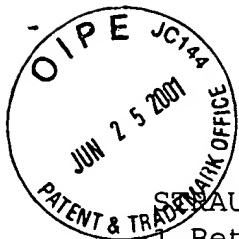
The applicants respectfully request that the following references listed on the attached PTO-FORM-1449 be considered in the examination of the above-identified application. A copy of each of these references is enclosed.

The applicants preserve the right to establish that any of the references listed on the attached PTO-FORM-1449 are not prior art to the above-captioned application.

Respectfully submitted,

Dated: June 20, 2001


John C. Pokotylo, Attorney
Reg. No. 36,242
Customer No. 26479
(732) 335-1222



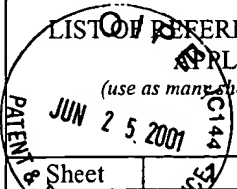
SEMAUB & POKOTYLO
1 Bethany Road
Suite 83, Bldg. 6
Hazlet, New Jersey 07730

CERTIFICATE OF MAILING under 37 C.F.R. 1.8(a)

I hereby certify that this correspondence is being deposited on **June 20, 2001** with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to the Assistant Commissioner for Patents, **Box Patent Application**, Washington, D.C. 20231.

John C. Pokotylo
John C. Pokotylo

36,242
Reg. No.

U.S. Department of Commerce Patent and Trademark Office		<i>Complete if Known</i>	
		Application Number: 09/872,892 Filing Date: June 1, 2001 First Named Inventor: Hung-Hsiang Jonathan CHAO Group Art Unit: Not yet assigned Examiner Name: Not yet assigned	
Sheet	1	of	1
		Attorney Docket No.: Poly-19/APP	

OTHER REFERENCES - NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume, issue number(s), publisher, country, where published, source	T ²
	AA.	N. W. McKeown, "Scheduling Algorithms for Input-Queued Cell Switches", PhD Thesis, University of California at Berkeley, (1995).	
	AB.	C. Y. Lee and A. Y. Oruc, "A Fast Parallel Algorithm for Routing Unicast Assignments in Benes Networks", <u>IEEE Trans. on Parallel and Distributed Sys.</u> , Vol. 6, No. 3, pp. 329-333 (March 1995).	
	AC.	T. T. Lee and S-Y Liew, "Parallel Routing Algorithms in Benes-Clos Networks", <u>Proc. IEEE INFOCOM '96</u> , pp. 279-286 (1996).	
	AD.	N. McKeown, M. Izzard, A. Mekittikul, W. Ellersick and M. Horowitz, "Tiny-Tera: A Packet Switch Core", <u>IEEE Micro.</u> , pp. 26-33 (Jan-Feb. 1997).	
	AE.	T. Chaney, J. A. Fingerhut, M. Flucke, J. S. Turner, "Design of a Gigabit ATM Switch", <u>Proc. IEEE INFOCOM '97</u> , PP. 2-11 (April 1997).	
	AF.	F. M. Chiussi, J. G. Kneuer, and V. P. Kumar, "Low-Cost Scalable Switching Solutions for Broadband Networking: The ATLANTA Architecture and Chipset", <u>IEEE Commun. Mag.</u> , pp. 44-53 (Dec. 1997).	
	AG.	J. Turner and N. Yamanaka, "Architectural Choices in Large Scale ATM Switches", <u>IEICE Trans. Commun.</u> , Vol. E81-B, No. 2, pp. 120-137 (Feb. 1998).	
	AH.	H. J. Chao and J-S Park, "Centralized Contention Resolution Schemes for a Large-Capacity Optical ATM Switch", <u>Proc. IEEE ATM Workshop '97</u> , (Fairfax, VA, May 1998).	
	AI.	N. McKeown, "The iSLIP Scheduling Algorithm for Input-Queued Switches", <u>IEEE/ACM Transactions on Networking</u> , Vol. 7, No. 2, (April 1999).	
	AJ.	N. McKeown, A. Mekittikul, V. Anantharam, and J. Walrand, "Achieving 100% Throughput in an Input-Queued Switch", <u>IEEE Trans. on Communications</u> , Vol. 47, No. 8, pp. 1260-1267 (Aug. 1999).	
	AK.	E. Oki, N. Yamanaka, Y. Ohtomo, K. Okazaki and R. Kawano, "A 10-Gb/s (1.25 Gb/s x 8) 4 x 2 0.25- μ m CMOS/SIMOX ATM Switch Based on Scalable Distributed Arbitration", <u>IEEE J. of Solid-State Circuits</u> , Vol. 34, No. 12, pp. 1921-1934 (Dec. 1999).	
	AL.	J. Chao, "Saturn: A Terabit Packet Switch Using Dual Round-Robin", <u>IEEE Communications Magazine</u> , pp. 78-84, (Dec. 2000).	
	AM.	E. Oki, Z. Jing, R. Rojas-Cessa, J. Chao, "Concurrent Round-Robin Dispatching Scheme in a Clos-Network Switch", <u>IEEE ICC 2001</u> , pp. 106-112, (June 2001).	

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Unique citation designation number. 2 Applicant is to place a check mark here if English language translation is attached.